WHAT IS CLAIMED IS:

1. A chip structure, comprising:

a semiconductor substrate having a plurality of electronic devices positioned on or in a surface layer of said semiconductor substrate;

a fine-line interconnection scheme comprising:

a plurality of dielectric layers over said semiconductor substrate, said dielectric layers having a plurality of via holes; and

a plurality of circuit layers each on one of said dielectric layers, wherein said circuit layers are electrically connected to each other through said via holes and are electrically connected to said electronic devices;

a passivation layer over said fine-line interconnection scheme, wherein said passivation layer comprises at least a opening exposing portion of the most top circuit layer;

a post-passivation scheme over said passivation layer and electrically connected to said circuit layers, wherein said post-passivation scheme comprises at least a bump pad and at least a testing pad, said testing pad electrically connecting to said bump pad; and

at least a bump over said bump pad.

2. The chip structure of Claim 1, wherein said post-passivation scheme comprising at least one metal layer, wherein said metal layer is a composite structure comprising an adhesion/barrier layer at the bottom and a gold layer at the top, said gold layer having a thickness greater than 1 μm.

3. The chip structure of Claim 2, wherein said adhesion/barrier layer consisting of material selected from a group of chromium, titanium, tantalum, titanium-tungsten alloy,

tantalum nitride and titanium-nitride.

4. The chip structure of Claim 1, wherein said post-passivation scheme comprising at least one metal layer, and wherein said metal layer is a composite structure comprising an adhesion/barrier layer and a copper layer; said copper layer formed on top of said adhesion/barrier layer.

5. The chip structure of Claim 4, wherein the material constituting said adhesion/barrier layer is selected from a group consisting of chromium, titanium, tantalum, titanium-tungsten alloy, titanium nitride and tantalum nitride.

6. The chip structure of Claim 4, wherein said metal layer further comprises a nickel layer formed on top of said copper layer.

7. The chip structure of Claim 6, wherein said metal layer further comprises a gold layer formed on top of said nickel layer.

8. The chip structure of Claim 1, wherein said post-passivation scheme comprises at least a metal layer and a polymer layer disposed between said metal layer and said passivation layer.

9. The chip structure of Claim 8, wherein said polymer layer is polyimide, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.

10. The chip structure of Claim 1, wherein said post-passivation scheme comprises at least a metal layer and a polymer layer covering said metal layer, said polymer layer having a plurality of openings exposing said testing pad or said bump pad.

11. The chip structure of Claim 10, wherein said polymer layer is polyimide, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.

12. The chip structure of Claim 1, wherein said post-passivation scheme comprises more than one metal layers.

13. The chip structure of Claim 1, wherein said post-passivation scheme comprising a top metal layer; wherein said top metal layer comprises at least a metal line connecting the bump pad to the testing pad.

14. The chip structure of Claim 1, wherein one of said circuit layers under the passivation layer comprises at least a metal line, and said bump pad is electrically connected to said testing pad through said metal line.

15. The chip structure of Claim 1, wherein said opening of the passivation layer has a width larger than about 0.1 μm.

16. The chip structure of Claim 1, wherein said passivation layer has a thickness larger than 0.35 μm.

17. The chip structure of Claim 1, wherein said passivation layer is a silicon-oxide layer, a silicon-nitride layer, a phosphosilicate glass (PSG) layer, a silicon-oxide-nitride layer or a composite structure comprising the above-mentioned layers.

18. The chip structure of Claim 1, wherein said post-passivation scheme comprises at least a top metal layer, wherein said top metal layer having a thickness larger than 0.4 μm.

19. The chip structure of Claim 1, wherein said bump comprises a solder metal and an under-bump-metallurgy layer, said under-bump-metallurgy layer is disposed on said bump pad and said solder metal is disposed on said under-bump-metallurgy layer.

20. The chip structure of Claim 19, wherein said under-bump-metallurgy layer is formed, from the bottom to the top, from a titanium layer, a copper layer, and a nickel layer.

21. The chip structure of Claim 19, wherein a material constituting the solder metal is selected from a group consisting of a tin-lead solder alloy and a lead-free solder alloy.

22. The chip structure of Claim 1, wherein said testing pad, after a testing step, is connected to a conductive wire by a wirebonding process. .

23. The chip structure of Claim 1, wherein post-passivation scheme comprises at least a wire-bonding pad and said wire-bonding pad is connected to a conductive wire by a wirebonding process.

24. . The chip structure of Claim 23, wherein said wire-bonding pad is electrically connected to said testing pad and/or said bump pad.

25. The chip structure of Claim 1, wherein the distance between said bump pad and said testing pad is smaller than 300 μm.

26. The chip structure of Claim 1, wherein the distance between said bump pad and said testing pad is smaller than 1 millimeter.

27. A chip structure, comprising:

a semiconductor substrate having a plurality of electronic devices positioned on or in a surface layer of said semiconductor substrate;

a fine-line interconnection scheme comprising:

a plurality of dielectric layers over said semiconductor substrate and said dielectric layers having a plurality of via holes; and

a plurality of circuit layers each on one of said dielectric layers, wherein said circuit layers are electrically connected to each other through said via holes and are electrically connected to said electronic devices;

a passivation layer over said fine-line interconnection scheme, wherein said

passivation layer comprises at least a opening exposing one of said circuit layer;

a post-passivation scheme over said passivation layer, wherein said post-passivation scheme comprises at least a metal layer electrically connected to said circuit layers, wherein said metal layer comprises a gold layer having a thickness larger than 1 μm and said metal layer comprises at least a bump pad and at least a wire-bonding pad;

at least a bump disposed on said bump pad; and

at least a conductive wire connected to said wire-bonding pad by a wirebonding process.

28. The chip structure of Claim 27, wherein said metal layer further comprises an adhesion/barrier layer underlying said gold layer.

29. The chip structure of Claim 28, wherein said material constituting said adhesion/barrier layer is selected from a group consisting of chromium, titanium, tantalum, titanium-tungsten alloy, tantalum nitride and titanium-nitride.

30. The chip structure of Claim 27, wherein said post-passivation scheme further comprises a polymer layer disposed between said metal layer and said passivation layer.

31. The chip structure of Claim 30, wherein said polymer layer is made of polyimide, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.

32. The chip structure of Claim 27, wherein said post-passivation scheme further comprises a polymer layer covering said metal layer.

33. The chip structure of Claim 32, wherein said polymer layer is made of polyimide, benzocyclobutene, porous dielectric material, parylene, epoxy, solder mask material or elastomer.

34. The chip structure of Claim 27, wherein said post-passivation scheme further

comprises a plurality of metal layers.

35. The chip structure of Claim 27, wherein said metal layer comprises at least a testing pad and at least a metal line and said metal line connects said bump pad to said testing pad.

36. The chip structure of Claim 27, wherein said metal layer comprises at least a testing pad and one of said circuit layers under said passivation layer comprises at least a metal line, said bump pad electrically connected to said testing pad through said metal line.

37. The chip structure of Claim 27, wherein said opening of said passivation layer has a width larger than about 0.1 um.

38. The chip structure of Claim 27, wherein said passivation layer has a thickness larger than 0.35 μm.

39. The chip structure of Claim 27, wherein said passivation layer is a silicon-oxide layer, a silicon-nitride layer, a phosphosilicate glass (PSG) layer, a silicon-oxide-nitride layer or a composite structure comprising said above-mentioned layers.

40. The chip structure of Claim 27, wherein said metal layer has a thickness larger than 0.4 μm.

41. The chip structure of Claim 27, wherein said bump comprises a solder metal and an under-bump-metallurgy layer, said under-bump-metallurgy layer is disposed on said bump pad and said solder metal is disposed on said under-bump-metallurgy layer.

42. The chip structure of Claim 41, wherein said under-bump-metallurgy layer is formed, from the bottom to the top, from a titanium layer, a copper layer and a nickel layer.

43. The chip structure of Claim 41, wherein a material constituting said solder

metal is selected from a group consisting of a tin-lead alloy and a lead-free solder alloy.

44. The chip structure of Claim 27, wherein said metal layer further comprises at least a testing pad electrically connected to said bump pad and the distance between said bump pad and said testing pad is smaller than 300 μm.

45. The chip structure of Claim 27, wherein said metal layer further comprises at least a testing pad electrically connected with said bump pad and the distance between said bump pad and said testing pad is smaller than 1 millimeter.